

Strain-Gated Piezotronic Logic Nanodevices

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A self-powered^[1] autonomous intelligent nanoscale system should consist of ultrasensitive nanowire (NW) based sensors,^[2–5] integrated high-performance memory and logic computing components for data storage and processing as well as decision making,^[6–12] and an energy scavenging unit for sustainable, self-sufficient, and independent operation.^[1,13–20] The existing semiconductor NW logic devices are based on electrically-gated field-effect transistors, which function as both the drivers and the active loads of the logic units by adjusting the conducting channel width.^[22,23] Moreover, the currently existing logic units are “static” and are almost completely triggered or agitated by electric signals, while the “dynamic” movable mechanical actuation is carried out by another unit possibly made of different materials.

Here, we present the first piezoelectric triggered mechanical-electronic logic operation using the piezotronic effect, through which the integrated mechanical electrical coupled and controlled logic computation is achieved using only ZnO NWs. By utilizing the piezoelectric potential created in a ZnO NW under externally applied deformation, strain-gated transistors (SGTs) have been fabricated, using which universal logic components such as inverters, NAND, NOR, XOR gates have been demonstrated for performing piezotronic logic calculations, which have the potential to be integrated with the NEMS technology for achieving advanced and complex functional actions in applications of vital importance in portable electronics, medical sciences and defense technology, such as in nanorobotics for sensing and actuating, in microfluidics^[24] for controlling the circuitry of the fluid flow, in other micro/nano-systems for intelligent control and action.

ZnO is unique because of its coupled piezoelectric and semiconductor properties, which is the piezotronic effect dealing with the piezoelectric potential (piezopotential) tuned/gated charge carrier transport process in a semiconductor material.^[25–27] The piezopotential created inside a ZnO NW under strain can be effectively used as a gate voltage, which has been applied for fabricating a range of piezotronic nanodevices,^[26,28] and therefore, the mechanic-electrical coupled and controlled actions can be performed in one structure unit made of a single material. Mechanical straining can create a piezopotential inside ZnO due to the polarization of the non-mobile ions, owing to the piezoelectric effect. In addition, the piezo-potential can act as a “controller” for gating the transport behavior of the charge carriers, which is the fundamental principle for strain

gated electronic devices, based on which ZnO-NW electromechanical switch has been fabricated.^[28]

A strain gated transistor (SGT) is made of a single ZnO NW with its two ends, which are the source and drain electrodes, being fixed by metal contact on a polymer substrate (Figure 1a). Once the substrate is bent, a tensile/compressive strain is created in the NW since the mechanical behavior of the entire structure is determined by the substrate. Utilizing the piezopotential created inside the NW, the gate input for a NW SGT is an externally-applied strain rather than an electrical signal. I_{DS} - V_{DS} characteristic for each single ZnO-NW SGT is obtained as a function of the strain created in the SGT (Figure 1a) before further assembly into logic devices. A NW SGT is defined as forward biased if the applied bias is connected to the drain electrode (Figure 1a).

For a SGT, the external mechanical perturbation induced strain (ϵ_g) acts as the gate input for controlling the “on”/“off” state of the NW SGT. The positive/negative strain is created when the NW is stretched/compressed (see SI for the calculation of the strain in the NW SGT). The I_{DS} - ϵ_g curves at a fixed V_{DS} show that I_{DS} increases as the gate strain ϵ_g increases and the threshold gate strain ϵ_T is around 0.08% (Figure 1b), which show that the SGT behaves in a similar way to a n -channel enhancement-mode MOSFET. The threshold gate strain ϵ_T is determined from the intercept (on the ϵ_g axis) of the tangent of the maximum slope region (shown as the black dashed line in Figure 1b) of the I_{DS} - ϵ_g curve. The I_{DS} - ϵ_g transfer curve obtained for drain bias voltage $V_{DS} = 1$ V (Figure S1) demonstrates that the NW SGT has a peak pseudo transconductance, $g_m = dI_{DS}(V_{DS})/d\epsilon_g$, which is 6 μ A for a strain change of $\Delta\epsilon_g = 1\%$. The on and off currents I_{on} and I_{off} for the NW SGT can be determined as the values obtained at $\epsilon_{g(off)} = \epsilon_T - 0.3\%$ and $\epsilon_{g(on)} = \epsilon_T + 0.7\%$, so that 70% of the ϵ_g swing above the threshold strain ϵ_T turns the ZnO NW SGT on, while the remaining 30% defines the “off” operation range, which is demonstrated in Figure S1. $I_{on} = 3.38$ μ A and $I_{off} = 0.03$ μ A are hence obtained with I_{on}/I_{off} ratio of 112 for $V_{DS} = 1$ V; this ratio is comparable to the reported value for the Ge/Si NW based device that was electrically driven.^[22] It can also be foreseen from the I_{DS} - ϵ_g transfer curves (Figure S1) that the ZnO-NW SGT based electromechanical amplifier can be realized by integrating with nanoscale electromechanical transducing units.^[6]

The working principle of a SGT is illustrated by the band structure of the device. A strain free ZnO NW have Schottky contacts at the two ends with the source and drain electrodes but with different barrier heights of Φ_S and Φ_D , respectively (Figure 1c1). The Fermi level inside the ZnO NW is considered flat here for illustration purpose, which is valid in our devices since the most majority of the bias falls at the reversed biased junction.^[28] When the drain is forward biased, the quasi-Fermi levels at the source ($E_{F,S}$) and drain ($E_{F,D}$) are different by the value of eV_{bias} , where V_{bias} is the applied bias (Figure 1c2). An

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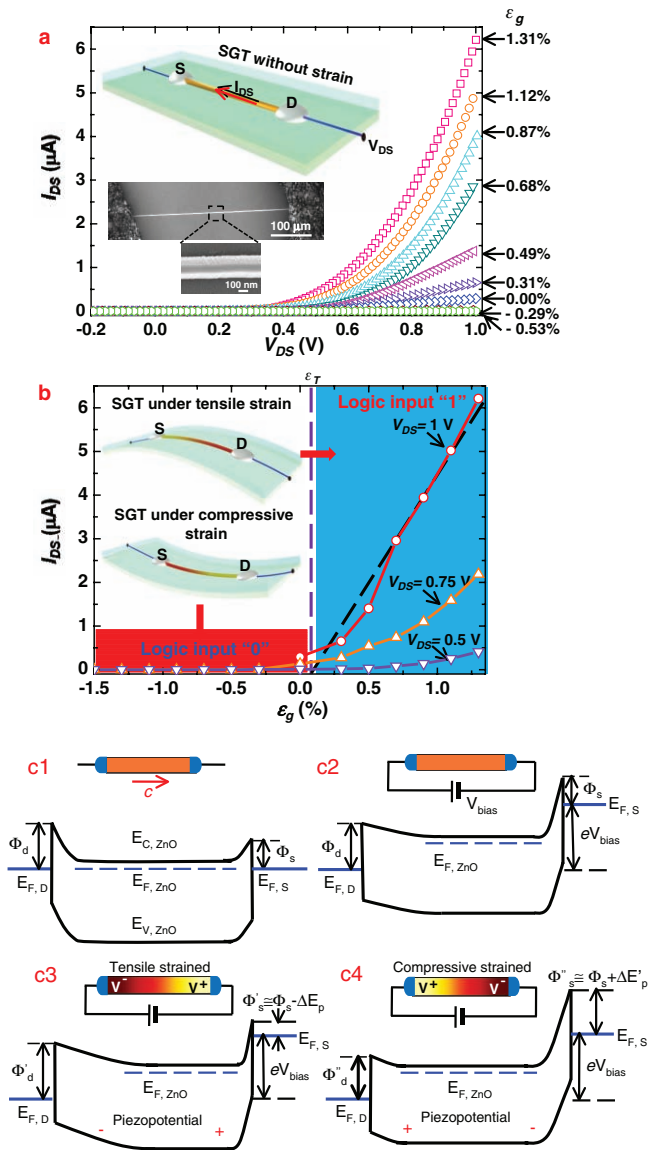


Figure 1. Single ZnO NW strain-gated transistor (SGT). a) I_{DS} - V_{DS} output characteristic for a ZnO SGT device with strain sweeping from $\epsilon_g = -0.53\%$ to 1.31% at a step of 0.2% . (Insets) Top, schematic of a single ZnO NW SGT under bias without strain. Current flows from drain to source electrode with external bias applied at the drain side. Bottom, top-view SEM image of the active part of a ZnO SGT ($L = 70 \mu\text{m}$, diameter = 300 nm), with both ends of the ZnO NW fixed by silver paste. b) I_{DS} - ϵ_g transfer characteristic for the same ZnO SGT device under three different V_{DS} bias values: 1 V , 0.75 V and 0.5 V , respectively. The threshold gate strain ϵ_T is determined as around 0.08% from the intercept (on the ϵ_g axis) of the tangent of the maximum slope region (shown as the black dashed line) of the I_{DS} - ϵ_g curve. (Insets) Top, schematic of a ZnO SGT under tensile strain and the corresponding I_{DS} - ϵ_g characteristic curve (blueish region), which is the logic "1" strain input region for the SGT. Bottom, schematic of a ZnO SGT under compressive strain and the corresponding I_{DS} - ϵ_g characteristic curve (red region), which is the logic "0" strain input region of the SGT. As in the NW, the piezopotential created by strain is negative in the red color region and positive in the yellow color region. c) The band structures of the ZnO NW SGT under different conditions for illustrating the mechanism of SGT. The crystallographic c -axis of the nanowire directs from drain to source. c1) The band structure of a strain-free ZnO NW SGT at equilibrium with different barrier heights

externally applied mechanical strain (ϵ_g) results in both the band structure change and piezoelectric potential field inside a ZnO NW.^[28] The change in band structure leads to the piezoresistance effect, which is a non-polar and symmetric effect at both the source and drain contacts. Since ZnO is a polar structure along c -axis, straining in axial direction (c -axis) creates a polarization of cations and anions in the NW growth direction, resulting in a piezopotential drop from V^+ to V^- inside the NW (Figure 1c), which produces an asymmetric effect on the changes in the Schottky barrier heights (SBHs) at the drain and source electrodes. Under tensile strain, the SBH at the source side reduces from Φ_S to $\Phi'_S \equiv \Phi_S - \Delta E_P$ (Figure 1c3), where ΔE_P denotes the change from the locally created piezopotential and it is a function of the applied strain, resulting in increased I_{DS} . For the compressively strained SGT, the sign of the piezopotential is reversed, and thus the SBH at the source side is raised from Φ_S to $\Phi''_S \equiv \Phi_S + \Delta E'_P$ (Figure 1c4), where $\Delta E'_P$ denotes the piezopotential effect on the SBH at source side, resulting in a large decrease in I_{DS} . Therefore, as the strain ϵ_g is swept from compressive to tensile regions, the I_{DS} current can be effectively turned from "off" to "on" while V_{DS} remains constant. This is the fundamental operating principle of the SGT.

The piezotronic strain-gated complementary logic gates are built using back-to-back packaged n -type ZnO NW SGTs on the top and bottom surfaces of a flexible substrate. Our first example is to illustrate the ZnO-NW strain-gated inverter (SGI) (Figure 2). When the substrate is bent downward (Figure 2a1), a tensile strain of 0.05 – 1.5% is created in SGT 1, while a compressive strain with the same magnitude is simultaneously produced in SGT 2, which results in a complementary "on" and "off" status in the two SGTs, respectively. Alternatively, if the substrate is bent upward (Figure 2a3), the two SGTs have a complementary "off" and "on" status, respectively. Therefore, these two SGTs behave in a similar way to the operation of the NMOS and PMOS transistors in the conventional complementary-metal-oxide-semiconductor (CMOS) inverters.^[29]

The strain-voltage transfer characteristic (SVTC) and noise margins of the NW SGI are obtained by plotting the measured output voltages versus corresponding gate strains (Figure 2b). V_{OH} and V_{OL} represent the high and low output voltages of the SGI, with ideal values of $V_{OH} = V_{DS} = 1 \text{ V}$ and $V_{OL} = 0 \text{ V}$. The experimental values for V_{OH} and V_{OL} are 0.98 V and 0.0001 V respectively. The smaller measured value for V_{OH} than the applied 1 V is due to the voltage drop across the SGT that is at "on" status. The logic swing of the SGI defined to be $(V_{OH} - V_{OL})$ is 0.98 V . The switching threshold strain of the SGI, ϵ_T , at which the output of the SGI switches between logic high and low status, is obtained at point C with strain value of -0.6% in Figure 2b. The slope value of the dashed line connecting the origin point and point C in Figure 2b is 1. In order to characterize

of Φ_S and Φ_D at the source and drain electrodes, respectively. c2) The quasi-Fermi levels at the source ($E_{F,S}$) and drain ($E_{F,D}$) of the ZnO SGT are split by the applied bias voltage V_{bias} . c3) With tensile strain applied, the SBH at the source side is reduced from Φ_S to $\Phi'_S \equiv \Phi_S - \Delta E_P$. c4) With compressive strain applied, the SBH at the source side is raised from Φ_S to $\Phi''_S \equiv \Phi_S + \Delta E'_P$. Corresponding changes in the SBHs at the drain side are indicated by Φ'_D and Φ''_D , deviating from Φ_D similar to those that occur at the source side in (c3) and (c4).

the effect of input gate strain on the SGI output, the largest input strain for generating output logic "1", ϵ_{IL} , and the smallest input strain for inducing output logic "0", ϵ_{IH} , are determined at the pseudo unit gain points A and B (see Figure 2b and S1) with strain values of -0.8% and -0.38% , respectively. The slopes of the SVTC curve (red line) at points A and B are both -1 . The input strain zone with $\epsilon < \epsilon_{IL}$ ($= -0.8\%$) (purple color zone in Figure 2b) induces the logic output of "1" for the SGI, while input strain zone with $\epsilon > \epsilon_{IH}$ ($= -0.38\%$) (the bluish color zone in Figure 2b) induces logic output "0" for the SGI. The negative values for ϵ_{IL} and ϵ_{IH} may be due to the fact that some initial strains were unpurposely introduced in the SGTs during the fabrication process.^[30] In the logic low input region (purple color region in Figure 2b), SGT 1 is on and SGT 2 is off; while in the logic high input region (blueish color region

in Figure 2b), SGT 1 is off and SGT 2 is on. The response time of the SGI is dictated by the straining rate, which is an application-dependent factor and the transient property can be investigated for ZnO NW SGI. The strain-gated logic devices are designed to interface with the ambient environment, which is associated with low-frequency mechanical actions, and the aim and targeting applications are different from those of conventional silicon devices which aim at speed. Switching frequency is not the critical issue as long as the strain-gated logic devices can respond to and process the mechanical signals in a timely manner, such as in applications of nanorobotics, transducers and micro-machine. The applications of SGTs are in complementary to those of the CMOS technology. Unlike conventional CMOS inverter, there is no electrical gate in the ZnO-NW SGT and hence the gate leakage current can be ignored in the ZnO-NW SGI. The temporal characteristics of current and voltage on a typical ZnO-NW SGI plotted against the same time-coordinate axis are shown in Figure S2.

Logic operations of NW strain-gated NAND and NOR gates were realized by integrating two NW SGIs, which are gated individually by the applied strains, according to corresponding connection rules (Figures 3a1 and 3a2 for NAND gate and Figure 3b1 and 3b2 for NOR gate). The output voltages of NAND and NOR gates versus the input gate strains are shown in Figures 3a3 for NAND gate and Figure 3b3 for NOR gate. Two types of transitions occur during the switching operation of both the ZnO NW strain-gated NAND and NOR gates, which have been tabulated (Tables S1 and Table S2). It can also be seen that NW strain-gated NAND and NOR gates with active loads (Figures 3a3 and 3b3) exhibit better overall performance, such as larger logic swing, compared to passive-load NAND and NOR gates (Figures 3c and 3d).

The strain-gated ZnO NW XOR logic was also realized by connecting two SGTs in parallel (Figure 4a). The drain electrode of SGT 1 in Figure 4a is connected to the electrical input V_A while the drain electrode of SGT 2 is connected to $V_{\bar{A}}$, which is the logically complement electrical input to V_A . If the strain gated input logic for SGT 2 is B, then the strain input logic for SGT 1 is \bar{B} . The change in the connections of the electrodes from those demonstrated in the NW SGI results in different logic functions. When the substrate is bent downward or upward, the electric output would be either V_A or $V_{\bar{A}}$, with the overall output of the device logically expressed as $V_{out} = \bar{B} V_A + B V_{\bar{A}}$, which is the XOR logic. The output voltages of the XOR gate versus the input gate strains are shown in Figure 4b.

If drain electrodes of SGT 1 and SGT 2 in Figure 4a are connected independently to arbitrary electrical input signals D_1 and D_0 rather than logically complements (V_A and $V_{\bar{A}}$), the XOR gate demonstrated above is essentially a 2:1 multiplexer (MUX), with a control bit B that is the input strain logic applied on SGT 2. Analogously, an n:1 MUX enables us to pick one of the n inputs and direct it to the output. When B is logic "1", SGT 1 is off and the output is determined by the input connected to the drain electrode of SGT 2. Conversely, when B is logic "0", SGT 2 is off and the output is determined by the input connected to the drain electrode of SGT 1. Reversely, if the inputs D_1 and D_0 act as the output ports and the output for MUX as the input side, the device acts as a demultiplexer (DEMUX). The circuit can be expanded easily to create larger MUXs based on the above

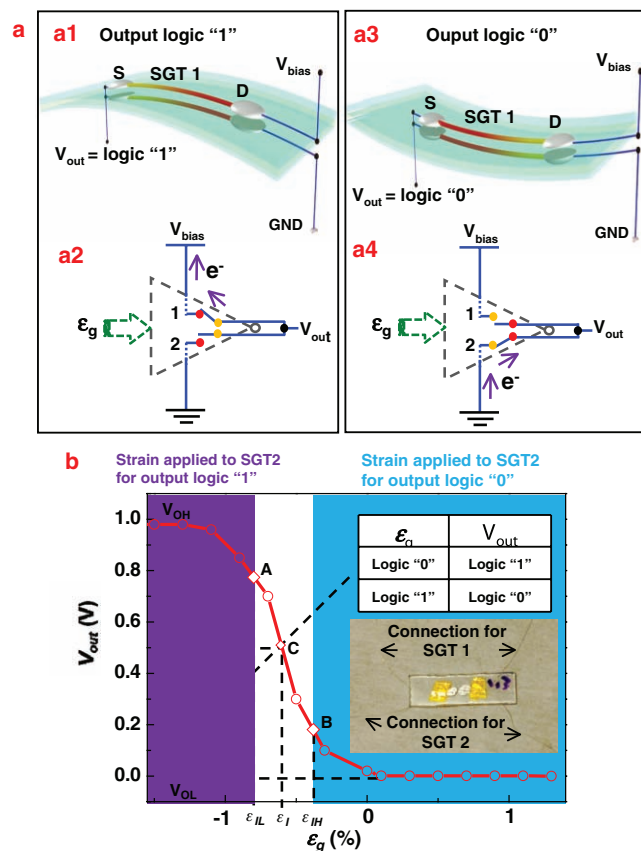


Figure 2. ZnO NW strain-gated inverter (SGI). a1-a4) Schematics and corresponding symbols of a ZnO NW SGI performing logic operations in responding input strain. The strain input for the SGI is defined in reference to the strain acting to SGT 2. When the strain input for the SGI is logic "0", SGT 1 is on and SGT 2 is off. Therefore the electrical output is logic "1" for the SGI. GND is the grounded end. When the strain input for the SGI is logic "1", SGT 1 is off and SGT 2 is on. Therefore the electrical output is logic "0" for the ZnO SGI. The x -axis direction and the polarity of the piezopotential field for each SGT under strains are defined in Figure 1. b) The strain-voltage transfer characteristic (SVTC) and noise margins of the ZnO NW SGI with $V_{DS} = 1$ V. The slope of the dashed line connecting the origin point and point C is 1. The slopes of points A and B on the SVTC curve (red line) are both -1 . Inset, optical picture of a ZnO NW SGI, with two SGTs and four connecting wires.

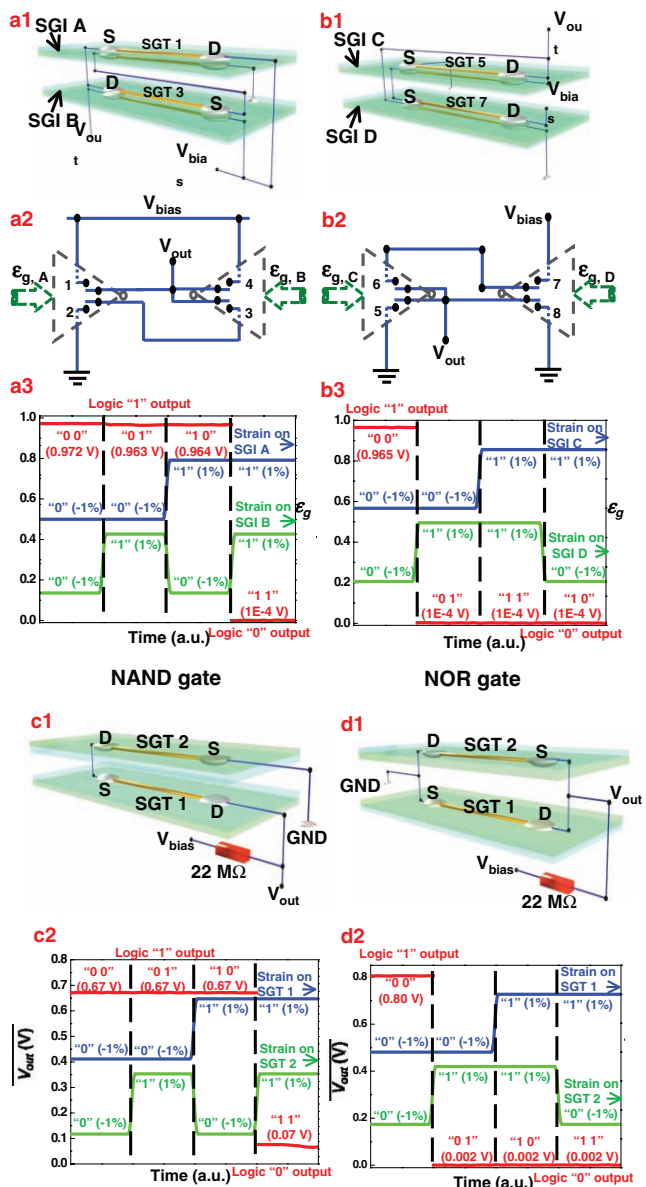


Figure 3. ZnO NW strain-gated NAND and NOR logic gates. a1–a3) ZnO NW strain-gated NAND gate. a1) Schematic of the ZnO NW strain-gated NAND logic gate, which is composed of two SGIs, SGI A and SGI B. The strain input A for SGI A is defined in reference to the strain applied to SGT 2 and the strain input B for SGI B is defined in reference to the strain applied to SGT 3. a2) Layout for ZnO NW strain-gated NAND logic gate by connecting two ZnO NW SGIs. a3) Logic operations and experimental truth table of the ZnO NW strain-gated NAND logic gate. Red line is the electrical output of the NAND gate. Blue and green lines represent the strain inputs applied on SGI A and SGI B respectively. “1” and “0” in the quotation marks along the input curves represent the logic levels of the inputs. For the output, the first number in the quotation marks represents the logic level for strain input on SGI A and the second number represents the logic level for strain input on SGI B. The values in the parenthesis are the corresponding physical values for the inputs and output. The same denominations apply for NOR and XOR logic gates. b1–b3) ZnO NW strain-gated NOR gate. b1) Schematic of the ZnO NW strain-gated NOR logic gate, which is composed of two SGIs, SGI C and SGI D. The strain input C for SGI C is defined in reference to the strain applied to SGT 5 and the strain input D for SGI D is defined in reference to the strain applied to SGT 7. b2) Layout for ZnO NW strain-gated NOR logic gate connecting two ZnO NW SGIs. b3) Logic operations and experimental truth table of the ZnO NW strain-gated NOR logic gate. Red line is the electrical output of the NOR gate. Blue and green lines represent the strain inputs applied on SGI C and SGI D, respectively. a.u., arbitrary units.

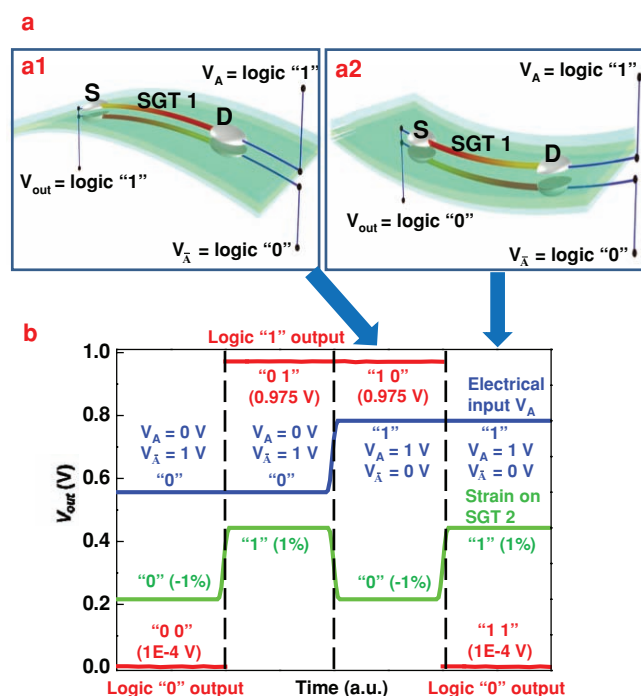


Figure 4. ZnO NW strain-gated XOR logic gate. a1–a2) Schematics of a ZnO NW XOR logic gate performing logic operations on strain and electrical inputs. a1) When the strain input applied on SGT 2 is logic “0” and the electrical input V_A applied on SGT 1 is logic “1”, SGT 1 is on and SGT 2 is off. Therefore the electrical output is logic “1” for the XOR gate. a2) When the strain input applied on SGT 2 is logic “1” and the electrical input V_A applied on SGT 1 is logic “0”, SGT 1 is off and SGT 2 is on. Therefore the electrical output is logic “0” for the XOR gate. b) Logic operations and experimental truth table of the ZnO NW strain-gated XOR logic gate. Red line is the electrical output of the XOR gate. Blue and green lines represent the electrical and strain inputs applied on SGT 1 and SGT 2, respectively. a.u., arbitrary units.

basic structures. The NW strain gated MUXs and DEMUXs are critical logic components for processing mechanic-electrical signals.

In summary, by utilizing the gating effect produced by piezoelectric potential in a ZnO NW under externally applied deformation, SGIs have been fabricated, using which the universal logic operations such as NAND, NOR and XOR gates have been

to the strain applied to SGT 8. b2) Layout for ZnO NW strain-gated NOR logic gate connecting two ZnO NW SGIs. b3) Logic operations and experimental truth table of the ZnO NW strain-gated NOR logic gate. Red line is the electrical output of the NOR gate. Blue and green lines represent the strain inputs applied on SGI C and SGI D, respectively. a.u., arbitrary units. c1) Schematic of a resistive-load ZnO NW NAND gate constructed from serial connection of two ZnO NWs. A 22 MΩ resistor is used as the pull-up load. c2) Logic operations and experimental truth table of the resistive-load ZnO NW NAND logic gate. Blue curve and green curve represent the strain inputs applied on SGT 1 and SGT 2, respectively. d1) Schematic of a resistive-load ZnO NW NOR gate constructed from parallel connection of two ZnO NWs. A 22 MΩ resistor is used as the pull-up load. d2) Logic operations and experimental truth table of the resistive-load ZnO NW NOR logic gate. Blue curve and green curve represent the strain inputs applied on SGT 1 and SGT 2, respectively.

demonstrated for the first time for performing piezotronic logic operations. In contrast to the conventional CMOS logic units, the SGT based logic units are driven by mechanical agitation and relies only on *n*-type ZnO NWs without the presence of *p*-type semiconductor components. The mechanical-electronic logic units can be integrated with NEMS technology to achieve advanced and complex functionalities in nanorobotics, microfluidics and micro/nano-systems. Recently, the integration of the other two important components in self-powered autonomous intelligent nanoscale system, the energy harvesting and the sensing/detecting parts, has been demonstrated^[31] and ZnO piezotronic logic devices can be further integrated with the ultrasensitive ZnO NW sensors and ZnO NW based nanogenerators to achieve a self-sustainable, all-nanowire-based, multifunctional self-powered autonomous intelligent nanoscale system.

Supporting Information

Supporting Information is available online from Wiley InterScience or from the author.

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- [1] Z. L. Wang, J. H. Song, *Science* **2006**, 312, 242.
 [2] F. Patolsky, G. F. Zheng, C. M. Lieber, *Nat. Protoc.* **2006**, 1, 1711.
 [3] Y. Cui, Q. Q. Wei, H. K. Park, C. M. Lieber, *Science* **2001**, 293, 1289.
 [4] E. Stern, J. F. Klemic, D. A. Routenberg, P. N. Wyrembak, D. B. Turner-Evans, A. D. Hamilton, D. A. LaVan, T. M. Fahmy, M. A. Reed, *Nature* **2007**, 445, 519.
 [5] P. H. Yeh, Z. Li, Z. L. Wang, *Adv. Mater.* **2009**, 21, 4975.
 [6] S. C. Masmanidis, R. B. Karabalin, I. De Vlaminck, G. Borghs, M. R. Freeman, M. L. Roukes, *Science* **2007**, 317, 780.
 [7] A. Bachtold, P. Hadley, T. Nakanishi, C. Dekker, *Science* **2001**, 294, 1317.
 [8] Y. Huang, X. F. Duan, Y. Cui, L. J. Lauhon, K. H. Kim, C. M. Lieber, *Science* **2001**, 294, 1313.
 [9] Z. H. Chen, J. Appenzeller, Y. M. Lin, J. Sippel-Oakley, A. G. Rinzler, J. Y. Tang, S. J. Wind, P. M. Solomon, P. Avouris, *Science* **2006**, 311, 1735.
 [10] C. Thelander, H. A. Nilsson, L. E. Jensen, L. Samuelson, *Nano Lett.* **2005**, 5, 635.
 [11] T. Rueckes, K. Kim, E. Joselevich, G. Y. Tseng, C. L. Cheung, C. M. Lieber, *Science* **2000**, 289, 94.
 [12] S. H. Lee, Y. Jung, R. Agarwal, *Nat. Nanotechnol.* **2007**, 2, 626.
 [13] M. S. Dresselhaus, G. Chen, M. Y. Tang, R. G. Yang, H. Lee, D. Z. Wang, Z. F. Ren, J. P. Fleurial, P. Gogna, *Adv. Mater.* **2007**, 19, 1043.
 [14] B. Z. Tian, X. L. Zheng, T. J. Kempa, Y. Fang, N. F. Yu, G. H. Yu, J. L. Huang, C. M. Lieber, *Nature* **2007**, 449, 885.
 [15] M. Law, L. E. Greene, J. C. Johnson, R. Saykally, P. D. Yang, *Nat. Mater.* **2005**, 4, 455.
 [16] X. D. Wang, J. H. Song, J. Liu, Z. L. Wang, *Science* **2007**, 316, 102.
 [17] Y. Qin, X. D. Wang, Z. L. Wang, *Nature* **2008**, 451, 809.
 [18] R. S. Yang, Y. Qin, L. M. Dai, Z. L. Wang, *Nat. Nanotechnol.* **2009**, 4, 34.
 [19] C. E. Chang, V. H. Tran, J. B. Wang, Y. K. Fuh, L. W. Lin, *Nano Lett.* **2010**, 10, 726.
 [20] C. F. Pan, H. Wu, C. Wang, B. Wang, L. Zhang, Z. D. Cheng, P. Hu, W. Pan, Z. Y. Zhou, X. Yang, J. Zhu, *Adv. Mater.* **2008**, 20, 1644.
 [21] K. L. Ekinci, M. L. Roukes, *Rev. Sci. Instrum.* **2005**, 76.
 [22] J. Xiang, W. Lu, Y. J. Hu, Y. Wu, H. Yan, C. M. Lieber, *Nature* **2006**, 441, 489.
 [23] P. Nguyen, H. T. Ng, T. Yamada, M. K. Smith, J. Li, J. Han, M. Meyyappan, *Nano Lett.* **2004**, 4, 651.
 [24] T. Thorsen, S. J. Maerkl, S. R. Quake, *Science* **2002**, 298, 580.
 [25] Z. L. Wang, *Adv. Funct. Mater.* **2008**, 18, 3553.
 [26] Z. L. Wang, *Mater. Sci. Eng. R* **2009**, 64, 33.
 [27] Nanopiezotronics was elected to be the top 10 emerging technologies by MIT Technology Review T10 in 2009: http://www.technologyreview.com/read_article.aspx?ch = specialsections&sc = tr10&id = 22118
 [28] J. Zhou, P. Fei, Y. D. Gu, W. J. Mai, Y. F. Gao, R. Yang, G. Bao, Z. L. Wang, *Nano Lett.* **2008**, 8, 3973.
 [29] P. E. Allen, D. R. Holberg, in *CMOS analog circuit design*, 2nd Ed., Oxford Univ. Press, Oxford, UK, **2002**.
 [30] Z. Y. Gao, J. Zhou, Y. D. Gu, P. Fei, Y. Hao, G. Bao, Z. L. Wang, *J. Appl. Phys.* **2009**, 106.
 [31] S. Xu, Y. Qin, C. Xu, Y. G. Wei, R. S. Yang, Z. L. Wang, *Nat. Nanotechnol.* **2010**, 5, 366.